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4. “Use It or Lose It: Proactive, Deterministic Longevity in Future Chip Multi-processors”, Siva Bhanu Krishna and Madhukar Reddy, TAMU.
5. “Pseudo Functional Path delay test through embedded Memories,” Yukun Gao, TAMU.
6. “Joint Precision Optimization and High Level Synthesis for Approximate Computing,” Chaofan Li, TAMU.
7. “At-Speed Path Delay Test,” Swati Chakraborty, TAMU.
8. “Unlock the LSIB with the FSM written in FPGA,” Yi Sun, SMU.
10. “Power-Efficient QoS for Application Specific Networks-on-Chip,” Hao He, TAMU.
11. “Smart Tuning of Analog Front-end for Key Sample Acquisition in Low Power Wearable Computers,” Qingxue Zhang, UT Dallas.
12. “Collaborative Gate Implementation Selection and Adaptivity Assignment for Robust Combinational Circuits,” Jiafan Wang, TAMU.
20. “Energy-Efficient Implementations of GF(p) and GF(2m) Elliptic Curve,” Andrew Targhetta, TAMU.
27. “A comparison of FinFET based FPGA LUT designs,” Monther Abusultan, TAMU.